Load Pull Characteristics of GaAs MESFETs Calculated Using an Analytic, Physics Based Large Signal Device Model

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ABSTRACT

The large signal nonlinear load pull characteristics of power GaAs MESFETs fabricated with uniform, ion-implanted, and lo-hi-lo doping profiles are calculated theoretically and compared. The calculation is performed using a load pull simulator in conjunction with a new physics based, analytic device model. The device and circuit models are interfaced using a harmonic balance routine.

INTRODUCTION

In recent years the rapid growth of the monolithic microwave integrated circuits (MMICs) market has spurred considerable interest in large signal modeling of GaAs MESFETs. An accurate computer-aided design (CAD) tool for the GaAs MESFET is important to the development of MMIC technology.

There are three empirical techniques presently used in the characterization of power FETs: 1) the load pull method [1], 2) 'large signal' S parameter measurements [2], and 3) characterization by means of small signal S parameters measured at different bias voltages [3]. These empirical methods all require that the device be fabricated prior to large signal characterization. Therefore, unless a systematic, controlled experiment on many devices is performed, little information can be gained from these techniques about the relation between large signal performance and device parameters.

In this work, a load pull algorithm has been developed and used in conjunction with a large signal, analytic device model [4] for the GaAs MESFET to theoretically calculate the large signal load pull characteristics of power FETs fabricated with uniform, ion-implanted, and lo-hi-lo channel doping profiles. A performance comparison of the three device types is presented. This technique permits systematic investigations of device designs before fabrication.

SIMULATION TECHNIQUE

The MESFET model used in this study is a physical model that describes the conduction and displacement currents of the FET as a function of device dimensions, material parameters, doping profile, bias conditions, and RF drive. The device model solves the basic semiconductor device equations in the time domain by an analytical technique. The device model is interfaced with a frequency domain circuit simulator by means of the harmonic balance method. The resulting simulator is capable of calculating the performance of various types of microwave circuits as a function of both device and circuit parameters.

The new load pull algorithm has been integrated into the simulator to produce a model that can be used to investigate load pull contours of GaAs MESFETs of various designs. The load pull algorithm functions by locating, using a quasi-Newton method, the conjugately matched load impedance for a specified input RF drive level and frequency. The output matching circuit is then detuned to achieve a desired reduction in output power, and points on each load pull contour are found using a secant method to find the length of vectors emanating at various angles from the conjugately matched load impedance. In this manner the entire load pull contour can be determined.

RF PERFORMANCE COMPARISON

The RF performance calculations were performed on GaAs MESFETs with doping profiles as illustrated in Fig. 1. The ion-implanted profile design is based upon an experimental device. The uniform doped and lo-hi-lo profile devices were designed to have the same charge in the channel under the gate as the ion-implanted device. All devices had gate lengths of 0.5 micron and gate widths of 1 mm. The load pull contours were calculated for each of the devices at a drain bias of 7 v

and bias currents of one half Idss and also near Idss. Operation near Idss will result in significant clipping of the RF voltage resulting in highly nonlinear performance. All calculations were performed at a frequency of 10 GHz.

The output power and gain versus input power characteristics for the three devices are shown in Figs. 2 and 3, respectively. For these particular designs the ion-implanted device produces the greatest linear and saturated output power and gain. When each device type is optimized for maximum performance, however, the uniform doped and lo-hi-lo profile device designs produce superior performance compared to the ion-implanted device.

LOAD PULL CALCULATIONS

The load pull contours were calculated for operation in both the linear and saturation regions. The results obtained for linear operation of the uniform doped device is shown in Fig. 4. For this calculation the device was biased at Idss/2 and was driven with 12 dbm input power. The load pull contours are essentially circles with relatively large diameters. The conjugate match point is on the real axis on the high impedance side of the chart. Increasing the input power to 24 dbm drives the device into saturation and the load pull contours shown in Fig. 5 result. The conjugate match point is forced to the low impedance side of the chart, but remains centered on the real axis. The diameter of the load pull contours is reduced and some distortion is observed in the shape of the contours. The contours are no longer circles and become elliptical. The distortion is due to waveform clipping and indicates the generation of harmonic signals.

The load pull contours for the ion-implanted device are shown in Figs. 6 and 7 for operation in the linear (Pin=12dbm) and saturation (Pin=30dbm) regions, respectively. The linear region operation again produces circular contours, although the conjugate match impedance is shifted to the inductive region of the Smith Chart. Driving the device into saturation again forces the conjugate match impedance to be essentially real and on the low impedance side of the chart. Distortion is again observed in the contours. Similar results were obtained for the lo-hi-lo profile device as shown in Figs. 8 and 9. Linear operation produces an inductive conjugate match impedance and large diameter circular contours. Increasing the input power forces the conjugate match impedance towards the real axis on the low impedance side of the chart. Operation in the saturation region distorts the load

pull contours and the contours become elliptical with reduced area relative to the linear operation contours. The reduction in the area of the contours is most likely due to increased losses in the device at high drive levels. This phenomenon would also account for the reduced input impedance of the devices.

CONCLUSIONS

A new load pull simulator has been developed and used to theoretically investigate the large signal performance of GaAs MESFETs of various designs. The load pull simulator shows that device operation in the linear region produces large diameter circular load pull contours. As the device is driven into saturation the input impedance of the device is forced to lower impedances and in the direction of increasing capacitance. The load pull contours become distorted and become elliptical with reduced area compared to the linear operation contours. The distortion is an indication of harmonic signal generation.

REFERENCES

1. Y. Takayama,"A New Load-Pull Characterization Method for Microwave Power Transistors," 1976 IEEE MTT-S International Microwave Symp. Digest, pp. 218-220.

2. R.S. Tucker,"RF Characterization of Microwave Power FETs," IEEE Trans. Microwave Theory and Tech., vol. MTT-29, pp. 776-781, Aug. 1981.

3. H.A. Willing, C. Raucher, and P. DeSantis,"A Technique for Predicting Large Signal Performance of a GaAs MESFET," IEEE Trans. Microwave Theory and Tech., vol. MTT-26, pp. 1017-1023, Dec. 1978.

4. M.A. Khatibzadeh and R.J. Trew,"A Large Signal Analytic Model for the GaAs MESFET," IEEE Trans. Microwave Theory and Tech., vol. MTT-36, pp. 231-238, Feb. 1988.
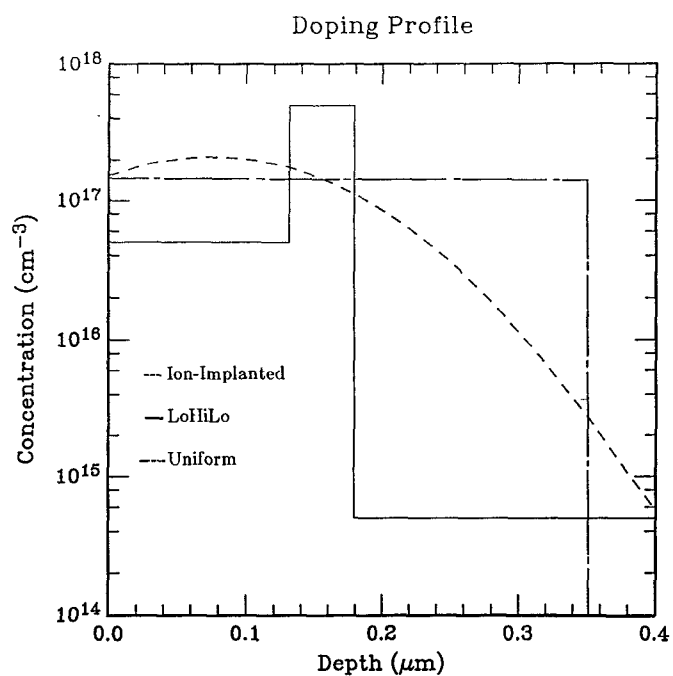
Doping Profile
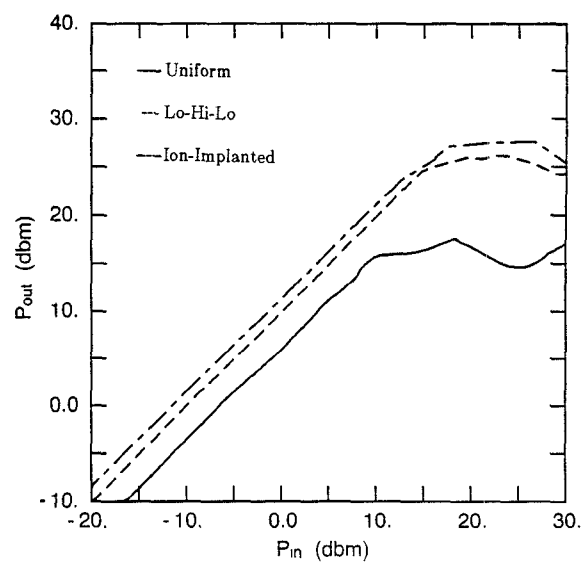

Fig. 1 GaAs MESFET Doping Profiles

Fig. 2 Power output versus Power Input

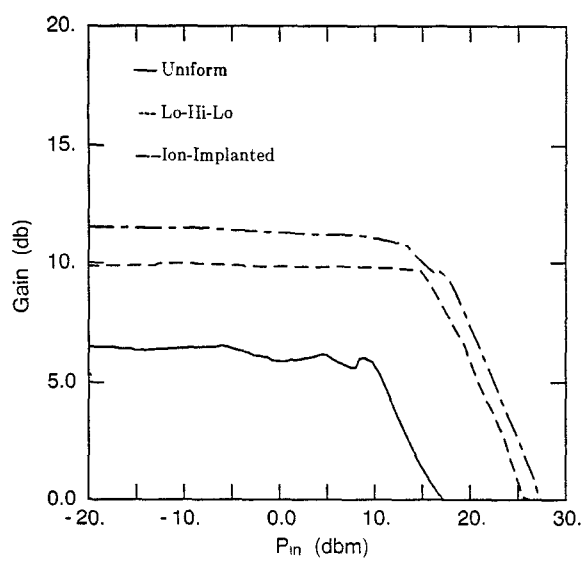**Fig. 3 Gain versus Power Input
for the Three Devices**

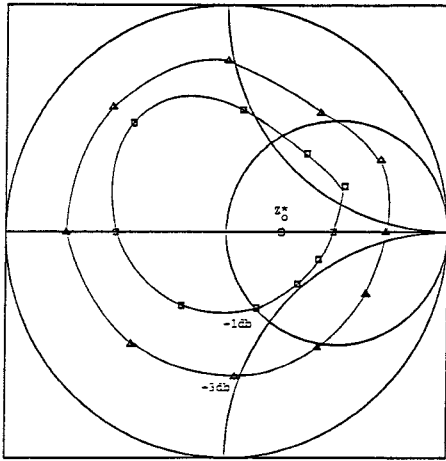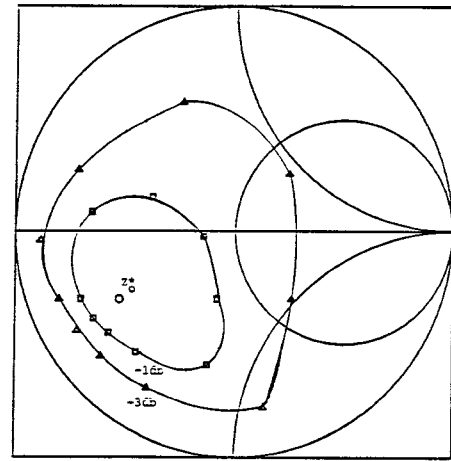Fig. 4 Load Pull Contours for the Uniform
Doped Device (Pin=12dbm, F=10 GHz)

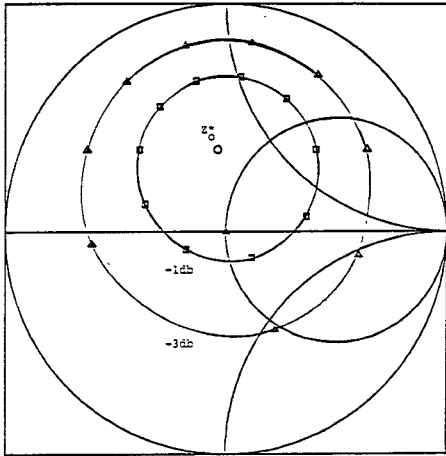Fig. 5 Load Pull Contours for the Uniform
Doped Device (Pin=24dbm, F=10 GHz)

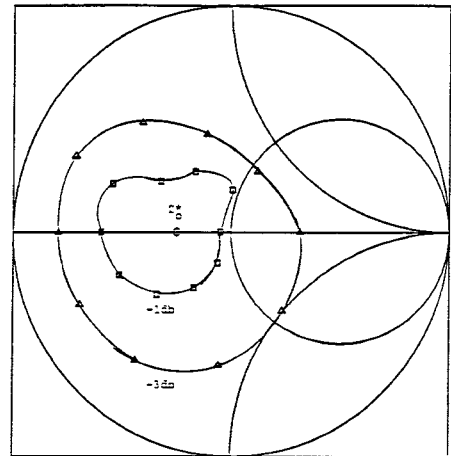Fig. 6 Load Pull Contours for the Ion-
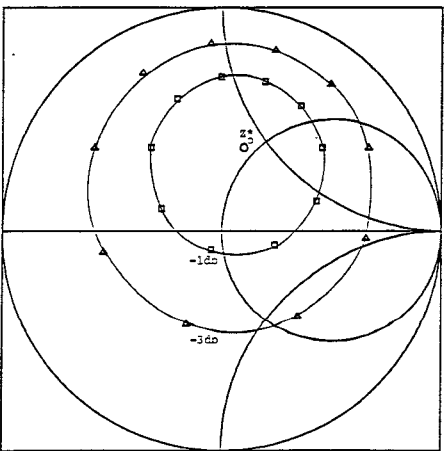Implanted Device (Pin=12dbm)

Fig. 7 Load Pull Contours for the Ion-
Implanted Device (Pin=30dbm)
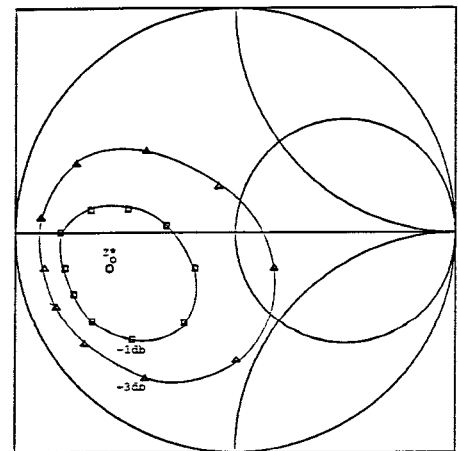
Fig. 8 Load Pull Contours for the Lo-Hi-Lo
Device (Pin=12dbm)

Fig. 9 Load Pull Contours for the Lo-Hi-Lo
Device (Pin=30dbm)

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